SENSE AMPLIFYING CIRCUIT AND BIT COMPARATOR WITH THE SENSE AMPLIFYING CIRCUIT

BACKGROUND OF THE INVENTION

[0001] This application claims the priority of Korean Patent Application No. 2003-12041, filed on February 26, 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

1. Field of the Invention

[0002] The present invention generally relates to a semiconductor circuit, and more particularly, to a sense amplifying circuit for detecting and amplifying differential signals with minutely different levels. The present invention also generally relates to a bit comparator employing such a sense amplifying circuit.

2. Description of the Related Art

[0003] General sense amplifying circuits are capable of synchronizing two differential signals with minutely different levels with a clock signal, sensing the synchronization signal, amplifying the sensed signal, and outputting the amplified signal.

[0004] FIG. 1 illustrates a conventional circuit diagram of a general amplifying circuit. The operation of a sense amplifying circuit 100 will be described with reference to FIG. 1. As is illustrated, two input signals INH and INL with minutely different levels may be applied to the sense amplifying circuit 100. In this case, the input signal INH has a higher voltage level than the input signal INL.

[0005] If a clock signal CLK is at a low level, precharge transistors PMP1 and PMP2 precharge first and second nodes N1 and N2, respectively, and NMOS transistors LMN1, LMN2, LM3, and LM4 are turned on.

[0006] If the clock signal CLK is transited to a high level, the sense amplifying circuit 100 starts a sensing operation with a switch transistor SWMN turned on. Although the precharge transistors PMP1 and PMP2 are turned on, latch

transistors LMP1 and LMP2 keep the first and second nodes N1 and N2 precharged.

[0007] Since an NMOS transistor SMN1 receiving the input signal INH allows a larger amount of current to flow than an NMOS transistor SMN2 receiving the input signal INL, a voltage level of the first node N1 is lower than a voltage level of the second node N2.

[0008] In other words, the first node N1 is at a low level, and the second node N2 is at a high level. Inverters I1 and I2 invert and output the voltage levels of the first and second nodes N1 and N2.

[0009] Accordingly, an output signal OUTH is output as a high level, and an output signal OUTL is output as a low level. As a result, there is an even larger difference between the voltage levels of the output signals OUTH and OUTL.

[0010] However, if a sense amplifying circuit should select and amplify one pair of differential signals from two pairs of differential signals, because the two pairs of differential signals are low-noise signals having a small swing, a general sense amplifying circuit generally must amplify both pairs and then select one pair. This may create a logic burden on a rear end of the sense amplifying circuit.

[0011] FIG. 2 illustrates a conventional circuit diagram of a general bit comparator.

[0012] The general bit comparator compares a tag value with address data input to a contents address memory (CAM) in a cache memory. The CAM is capable of storing data input from an external source, and comparing the stored data with address data input from an external source to determine whether the stored data coincides with the address data. The data stored in the CAM is generally called a tag, and the bit comparator compares the tag with input address data.

[0013] The operation of the general bit comparator will be explained with reference to FIG. 2. A data maintainer 230 has a latch structure in which input nodes of inverters ID1 and ID2 are connected to output nodes of the inverters ID1 and ID2, and receive and store data DATA and inverted data INDATA from a pair of bit lines BL and BLB via transistors CMN1 and CMN2 controlled by a word line WL. This value is a tag.

[0014]Assuming that the data DATA has a low level, the inverted data INDATA has a high level, and address data INH and INL that do not coincide with the data DATA and inverted data INDATA are input. In other words, the address data INH is at a high level, and the address data INL is at a low level.

[0015]The address data INH and INL is input to a driver 220 via a sense amplifying circuit 210 which operates in synchronicity with a clock signal CLK. The sense amplifying circuit 210 generally has the same structure as the general sense amplifying circuit 100 shown in FIG. 1, and the address data INH and INL is amplified through the sense amplifying circuit 210 and the driver 220.

[0016]When the data DATA and the inverted data INDATA is applied to transmission gates TG1 and TG2, respectively, the transmission gate TG1 is turned on, and the transmission gate TG2 is turned off. The address data INH with the high level is output as a match signal MATL via the transmission gate TG1. The address data INL with the low level is not output because the transmission gate TG2 is turned off.

[0017]Outputting the match signal MATL at a high level indicates that the address data INH and INL input to a bit comparator 200 may each have a different level from the data DATA and the inverted data INDATA. Outputting the match signal MATL at a low level indicates that the address data INH and INL input to the bit comparator 200 each have the same level as the data DATA and the inverted data INDATA.

[0018]A general bit comparator normally generates a match signal by amplifying input address data through a sense amplifying circuit and a driver, and comparing the input address data with stored data. As a result, a significant time is taken from the input of the address data to the output of the match signal. This is problematic in a cache memory which is required to operate at a high speed.

SUMMARY OF THE INVENTION

[0019] An exemplary embodiment of the present invention may provide a sense amplifying circuit capable of selecting one pair of two pairs of differential signals and amplifying the selected pair of differential signals.

[0020] An exemplary embodiment of the present invention is also capable of providing a bit comparator for operating at a high speed by including a sense amplifying circuit.

[0021] According to an exemplary embodiment of the present invention, a sense amplifying circuit my include a selecting unit for selecting one pair from a first pair of a first signal and a first inverted signal and a second pair of a second signal and a second inverted signal, the selecting unit selecting the one pair in response to a selection signal and an inverted selection signal; a sensing unit for sensing voltage levels of one pair of signals selected from the first pair and the second pair; a latching unit for precharging first and second nodes in response to a clock signal and for controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit; an output unit for inverts the voltage levels of the first and second nodes to generate first and second output signals; and a switching unit for controlling the operation of the selecting unit in response to the clock signal.

[0022] According to an exemplary embodiment of the present invention, a sense amplifying circuit may include a selecting unit for selecting one pair from a first pair of a first signal and a first inverted signal and a second pair of a second signal and a second inverted signal, in response to a first level of a clock signal, a selection signal, and an inverted selection signal; a sensing unit for sensing voltage levels of one pair of signals selected from the first and second pairs; a latching unit for precharging first and second nodes in response to a second level of the clock signal and controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit; and an output unit for inverting the voltage levels of the first and second nodes to generate first and second output signals.

[0023] According to an exemplary embodiment of the present invention, a bit comparator may include a random access memory cell for receiving and storing data and inverted data having an opposite level to the data from a pair of data lines to generate a selection signal and an inverted selection signal in response to a control signal; a selecting unit for selecting one pair from a first pair of first signal and first inverted signal and a second pair of second signal and second inverted signal in response to a first level of a clock signal, the selection signal, and the inverted selection signal; a sensing unit for sensing

voltage levels of one pair of signals selected from the first and second pairs; a latching unit for precharging first and second nodes in response to a second level of the clock signal and controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit; and an output unit for inverting the voltage levels of the first and second nodes to generate first and second output signals and determines in response to a level of the second output signal whether the data and the inverted data coincide with the first signal and the first inverted signal.

[0024] According to an exemplary embodiment of the present invention, an apparatus may include a selecting unit for selecting a signal pair from at least two pairs of signals, the selecting unit selecting the signal pair based upon at least one selection signal; and amplifying circuitry for amplifying only the pair selected from the at least two pairs of signals.

[0025] According to an exemplary embodiment of the present invention, a method includes selecting a signal pair from at least two pairs of signals based upon at least one selection signal; and amplifying only the signal pair selected from the at least two pairs of signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Exemplary embodiments of the present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

FIG. 1 illustrates a conventional circuit diagram of a general sense amplifying circuit;

FIG. 2 illustrates a conventional a circuit diagram of a general bit comparator;

FIG. 3 illustrates a circuit diagram of a sense amplifying circuit according to an exemplary embodiment of the present invention;

FIG. 4 illustrates is a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 3;

FIG. 5 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 3;

FIG. 6 illustrates a circuit diagram of a sense amplifying circuit according to another exemplary embodiment of the present invention;

FIG. 7 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 6;

FIG. 8 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 6;

FIG. 9 illustrates a circuit diagram of a bit comparator according to another exemplary embodiment of the present invention;

FIG. 10 illustrates a modified circuit diagram of the bit comparator of FIG. 9; and

FIG. 11 illustrates a block diagram for explaining the bit comparators of FIGS. 9 and 10.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0027] It may be useful to refer to the attached drawings in order to gain understanding of the merits of exemplary embodiments of the present invention, the operation thereof, and the objectives accomplished thereby. However, those of ordinary skill in the art appreciate the exemplary embodiments illustrated and described herein have been given by way of example only and may not be considered as limiting of the claimed invention.

[0028] Hereinafter, exemplary embodiments of the present invention will be explained with reference to the attached drawings. Like reference numerals denote like members throughout the drawings.

[0029] FIG. 3 illustrates a circuit diagram of a sense amplifying circuit according to an exemplary embodiment of the present invention. Referring to FIG. 3, a sense amplifying circuit 300 may include a selecting unit 310, a sensing unit 320, a latching unit 330, an output unit 340, and a switching unit 350.

[0030] The latching unit 330 may precharge first and second nodes N1 and N2 in response to a clock signal CLK and may control voltage levels of the first and second nodes N1 and N2 in response to a sensing result of the sensing unit 320.

[0031] In more detail, the latching unit 330 may include first and second precharge transistors PMP1 and PMP2, and first, second, third, fourth, fifth,

and sixth latch transistors LMP1, LMP2, LMN3, LMN4, LMN5, and LMN6. The first precharge transistor PMP1 has a first end connected to a power voltage VDD, a second end connected to a first node N1, and a gate connected to the clock signal CLK. The second precharge transistor PMP2 has a first end connected to the power voltage VDD, a second end connected to a second node N2, and a gate connected to the clock signal CLK. The first latch transistor LMP1 has a first end connected to the power voltage VDD, a second end connected to the first node N1, and a gate connected to the second node N2. The second latch transistor LMP2 has a first end connected to the power voltage VDD, a second end connected to the second node N2, and a gate connected to the first node N1. The third and fourth latch transistors LMN3 and LMN4 have first ends connected to the first node N1 and gates connected to the second node N2. The fifth and sixth latch transistors LMN5 and LMN6 have first ends connected to the second node N2 and gates connected to the first node N1.

[0032] The latching unit 330 may further include a first current pass transistor KMN1 which has a first end connected to the first node N1, a second end connected to the switching unit 350, and a gate connected to the second node N2, and a second current pass transistor KMN2 which has a first end connected to the second node N2, a second end connected to the switching unit 350, and a gate connected to the first node N1.

[0033] The sensing unit 320 is capable of sensing voltage levels of one pair of signals selected from a first pair of signals INH1 and INL1 and a second pair of signals IN2 and INL2. The sensing unit 320 includes first and second sense transistors MN1 and MN2, and first and second inverted sense transistors IMN1 and IMN2. The first sense transistor MN1 has a first end connected to the second end of the third latch transistor LMN3 and a gate connected to the first signal INH1. The first inverted sense transistor IMN1 has a first end connected to the second end of the sixth latch transistor LMN6 and a gate connected to the first inverted signal INL1. The second transistor MN2 has a first end connected to the second end of the fourth latch transistor LMN4 and a gage connected to the second signal INH2. The second inverted sense transistor IMN3 has a first end connected to the second end of

the fifth latch transistor LMN5 and a gate connected to the first inverted signal INL1.

[0034] The selecting unit 310 may select one pair from the first pair of first signal INH1 and first inverted signal INL1 and the second pair of second signal INH2 and inverted signal INL2 in response to a selection signal SEL and an inverted selection signal ISEL.

[0035] To be more specific, the selecting unit 310 may further include first and second select transistors SMN1 and SMN2. The first select transistor SMN1 has a first end connected to the second end of the first sense transistor MN1 and the second end of the first inverted sense transistor IMN1, a gate connected to the selection signal SEL, and a second end connected to a third node N3. The second select transistor SMN2 has a first end connected to the second end of the second sense transistor MN2 and the second end of the second inverted sense transistor IMN2, a gate connected to the inverted selection signal ISEL, and a second end connected to the third node N3.

[0036] The output unit 340 inverts voltage levels of the first and second nodes N1 and N2 to output first and second output signals OUTH and OUTL. The switching unit 350 controls the operation of the selecting unit 310 in response to the clock signal CLK.

[0037] The switching unit 350 may be a switch transistor SWMN which has a first end connected to the third node N3, a gate connected to the clock signal CLK, and a second end connected to a ground voltage VSS.

[0038] Hereinafter, the operation of the sense amplifying circuit 300 will be described with reference to FIG. 3.

[0039] Unlike the sense amplifying circuit 100 of FIG. 1, the sense amplifying circuit 300 of FIG. 3 receives two pairs of differential signals, i.e., a first pair of first signal INH1 and first inverted signal INL1 and a second pair of second signal INH2 and second inverted signal INL2. Since the sense amplifying circuit 300 according to an exemplary embodiment of the present invention selects and amplifies one of the two pairs of differential signals, no burden is generally imposed on a rear end of the sense amplifying circuit 300.

[0040] When the clock signal CLK is at a low level, the first and second precharge transistors PMP1 and PMP2 are turned on, the first and second

nodes N1 and N2 are precharged, and the third, fourth, fifth, and sixth transistors LMN3, LMN4, LMN5, and LMN6 are turned on.

[0041] When the clock signal CLK is transited to a high level, the switch transistor SWMN of the switching unit 350 is turned on. The selecting unit 310 selects one pair from the first pair of first signal INH1 and first inverted signal INL1 and the second pair of second signal INH2 and second inverted signal INL2 in response to the selection signal SEL and the inverted selection signal ISEL.

[0042] When the selection signal SEL has a high level, and the inverted signal ISEL has a low level, the first select transistor SMN1 is turned on, and the second select transistor SMN2 is turned off.

[0043] When the first select transistor SMN1 is turned on, the first sense transistor MN1 and the first inverted sense transistor IMN1 of the sensing unit 320 operate, and the second sense transistor MN2 and the second inverted sense transistor IMN2 of the sensing unit 320 do not operate. Accordingly, the first signal INH1 and the first inverted signal INL1 input to the gates of the first sense transistor MN1 and the first inverted sense transistor IMN1 are sensed, while the second signal INH2 and the second inverted signal INL2 are not sensed.

[0044] When the voltage level of the first signal INH1 is higher than the voltage level of the first inverted signal INL1, the third, fourth, fifth, and sixth latch transistors LMN3, LMN4, LMN5, and LMN6 are turned on. However, since the second sense transistor MN2 and the second inverted sense transistor IMN2 do not operate, the fourth and fifth latch transistors LMN4 and LMN5 do not operate.

[0045] In addition, since the voltage level of the first signal INH1 is higher than the voltage level of the first inverted signal INL1, the first sense transistor MN1 allows a larger amount of current to flow than the first inverted sense transistor IMN1. Thus, a voltage level of the first node N1 becomes lower than a voltage level of the second node N2.

[0046] The output unit 340 inverts the voltage levels of the first and second nodes N1 and N2 using inverters I1 and I2 to output first and second output signals OUTH and OUTL. The voltage level of the first output signal OUTH is higher than the voltage level of the second output signal OUTL.

Consequently, the first signal INH1 and the first inverted signal INL1 are amplified and output as the first and second output signals OUTH and OUTL.

[0047] In contrast, when the selection signal SEL has a low level and the inverted selection signal ISEL has a high level, the second sense transistor MN2 and the second inverted sense transistor IMN2 operate, and thus the second signal INH2 and the second inverted signal INL2 are amplified and output.

[0048] Accordingly, although two pairs of differential signals are input to the sense amplifying circuit 300, generally no burden is imposed on the rear end of the sense amplifying circuit 300.

[0049] FIG. 4 illustrates is a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 3.

[0050] A sense amplifying circuit 400 of FIG. 4 is substantially identical to the sense amplifying circuit 300 except that a selecting unit 410 has a different structure from the selecting unit 310.

[0051] The selecting unit 410 may include first and second select transistors SMN1 and SMN2, and first and second inverted select transistors ISMN1 and ISMN2. The first select transistor SMN1 has a first end connected to a second end of the first sense transistor MN1, a gate connected to a selection signal SEL, and a second end connected to a third node N3. The first inverted select transistor ISMN1 has a first end connected to a second end of the first inverted sense transistor IMN1, a gate connected to the selection signal SEL, and a second end connected to the third node N3. The second select transistor SMN2 has a first end connected to a second end of the second sense transistor MN2, a gate connected to an inverted signal ISEL, and a second end connected to the third node N3. The second inverted select transistor ISMN2 has a first end connected to a second end of the second inverted sense transistor IMN2, a gate connected to the inverted signal ISEL, and a second end connected to the third node N3.

[0052] The first select transistor SMN1 of the selecting unit 310 is connected to the first sense transistor MN1 and the first inverted sense transistor IMN1 to control the first sense transistor MN1 and the first inverted sense transistor IMN1.

[0053] The first sense transistor MN1 of the selecting unit 410 is controlled by the first select transistor SMN1, and the first inverted sense transistor IMN1 is controlled by the first inverted select transistor ISMN1. The second sense transistor MN2 is controlled by the second select transistor SMN2, and the second inverted sense transistor IMN2 is controlled by the second inverted select transistor ISMN2.

[0054] It is understood by those of ordinary skill in the art that the selecting unit 410 of FIG. 4 performs substantially the same functions as the selecting unit 310 illustrated in FIG. 3. Thus, the functions of the selecting unit 410 will not be explained herein.

[0055] First and second precharge transistors PMP1 and PMP2, and first and second latch transistors LMP1 and LMP2 are PMOS transistors. Third, fourth, fifth, and sixth transistors LMN3, LMN4, LMN5, and LMN6, the first and second sense transistors MN1 and MN2, the first and second inverted sense transistors IMN1 and IMN2, the first and second select transistors SMN1 and SMN2, the first and second inverted select transistors ISMN1 and ISMN2, and a switch transistor SWMN are NMOS transistors.

[0056] It is understood by those of ordinary skill in the art that a sense amplifying circuit may be constituted by changing PMOS transistors into NMOS transistors or NMOS transistors into PMOS transistors.

[0057] FIG. 5 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 3.

[0058] A sense amplifying circuit 500 of FIG. 5 is substantially the same as the sense amplifying circuit 400 except that a switching unit 550 has a different structure from the switching unit 450.

[0059] Referring to FIG. 5, unlike the switching unit 450, switch transistors SWMN1, SWMN2, SWMN3, and SWMN4 of the switching unit 550 are connected to first and second select transistors SMN1 and SMN2, and first and second inverted select transistors ISMN1, and ISMN2, respectively.

[0060] It is understood by those of ordinary skill in the art that the switching unit 550 of FIG. 5 performs substantially the same functions as the switching unit 450 of FIG. 4. Thus, the functions of the switching unit 550 will not be explained herein.

[0061] FIG. 6 illustrates a circuit diagram of a sense amplifying circuit according to another exemplary embodiment of the present invention.

[0062] Referring to FIG. 6, a sense amplifying circuit 600 may include a selecting unit 610, a sensing unit 620, a latching unit 630, and an output unit 640.

[0063] The latching unit 630 precharges first and second nodes N1 and N2 in response to a second level of a clock signal CLK and controls voltage levels of the first and second nodes N1 and N2 in response to a sensing result of the sensing unit 620.

[0064] The structure of the latching unit 630 is substantially the same as that of the latching unit 330 of the sense amplifying circuit 300 of FIG. 3 and thus will not be explained again.

[0065] The sensing unit 620 is capable of sensing voltage levels of one pair of signals selected from a first pair of first signal INH1 and first inverted signal INL1 and a second pair of second signal INH2 and second inverted signal INL2. The structure of the sensing unit 620 is substantially identical to that of the sensing unit 320 of the sense amplifying circuit 300 of FIG. 3 and thus will not be described again.

[0066] The selecting unit 610 is capable of selecting one pair from the first pair of first signal INH1 and first inverted signal INL1 and the second pair of second signal INH2 and second inverted signal INL2 in response to a first level of the clock signal CLK, a selection signal SEL, and an inverted signal ISEL.

[0067] In more detail, the selecting unit 610 may include first and second switch transistors SWMN1 and SWMN2, and first and second select transistors SMN1 and SMN2. The first switch transistor SWMN1 has a first end connected to a second end of a first sense transistor MN1 and a second end of a first inverted sense transistor IMN1, and a gate connected to the clock signal CLK. The second switch transistor SWMN2 has a first end connected to a second end of a second sense transistor MN2 and a second end of a second inverted sense transistor IMN2, and a gate connected to the clock signal CLK. The first select transistor SMN1 has a first end connected to a second end of the first switch transistor SWMN1, a gate connected to the selection signal SEL, and a second end connected to a ground voltage VSS.

The second select transistor SMN2 has a first end connected to a second end of the second switch transistor SWMN2, a gate connected to the inverted selection signal ISEL, and a second end connected to the ground voltage VSS.

[0068] The output unit 640 inverts the voltage levels of the first and second nodes N1 and N2 to output first and second output signals OUTH and OUTL.

[0069] The operation of the sense amplifying circuit 600 will be described with reference to FIG. 6.

[0070] The sense amplifying circuit 600 of FIG. 6 is different from the sense amplifying circuit 300 of FIG. 3 in positions of the first and second switch transistors SWMN1 and SWMN2 and the first and second select transistors SMN1 and SMN2. In other words, in the sense amplifying circuit 300, the first and second select transistors SMN1 and SMN2 are directly connected to the sensing unit 320, and the switch transistor SWMN is connected between the selecting unit 310 and the ground voltage VSS.

[0071] In contrast, in the sense amplifying circuit 600 of FIG. 6, the first and second switch transistors SWMN1 and SWMN2 are directly connected to the sensing unit 620, and the first and second select transistors SMN1 and SMN2 are connected to the ground voltage VSS.

[0072] When the clock signal CLK is at a low level, the latching unit 630 precharges the first and second nodes N1 and N2. When the clock signal CLK is transited to a high level, the first and second switch transistors SWMN1 and SWMN2 are turned on. For convenience, the high level of the clock signal CLK is called a first level and the low level of the clock signal CLK is called a second level.

[0073] When the first and second switch transistors SWMN1 and SWMN2 are turned on, the selection signal SEL with a high level and the inverted selection signal ISEL with a low level are input. Then, the first select transistor SMN1 is turned on, and the second select transistor SMN21 is turned off.

[0074] Although the second switch transistor SWMN2 is turned on, the second select transistor SMN2 is turned off. Thus, the second sense transistor MN2 and the second inverted sense transistor IMN2 to which the second signal INH2 and the second inverted signal INL2 are applied, respectively, do not operate, while the first sense transistor MN1 and the first inverted sense

transistor IMN1 to which the first signal INH1 and the first inverted signal INL1 are applied, respectively, operate.

[0075] When a voltage level of the first signal INH 1 is higher than a voltage level of the first inverted signal INL1, third, fourth, fifth, and sixth latch transistors LMN3, LMN4, LMN5, and LMN6 are turned on. However, since the second sense transistor MN2 and the second inverted sense transistor IMN2 do not operate, the fourth and fifth latch transistors LMN4 and LMN5 do not operate.

[0076] Since the voltage level of the first signal INH1 is higher than the voltage level of the first inverted signal INL1, the first sense transistor MN1 allows a larger amount of current to flow than the first inverted sense transistor IMN1. Then, the voltage level of the first node N1 is lower than the voltage level of the second node N2.

[0077] The output unit 640 inverts the voltage levels of the first and second nodes N1 and N2 using inverters I1 and I2 to output the first and second output signals OUTH and OUTL. A voltage level of the first output signal OUTH is higher than a voltage level of the second output signal OUTL. As a result, the first signal INH1 and the first inverted signal INL1 are amplified and output as the first and second output signals OUTH and OUTL, respectively.

[0078] When the selection signal SEL has a low level and the inverted signal ISEL has a low level, the second sense transistor MN2 and the second inverted sense transistor IMN2 operate. Thus, the second signal INH2 and the second inverted signal INL2 are amplified and output.

[0079] Accordingly, although two pairs of differential signals are input to the sense amplifying circuit 600 of FIG. 6, a significant burden is generally not imposed on the rear end of the sense amplifying circuit 600.

[0080] FIG. 7 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 6.

[0081] Referring to FIG. 7, first and second switch transistors SWMN1 and SWMN2, and first and second inverted switch transistors ISWMN1 and ISWMN2 are connected to first and second sense transistors MN1 and MN2, and first and second inverted sense transistors IMN1 and IMN2, respectively.

[0082] It is understood by those of ordinary skill in the art that a selecting unit 710 of FIG. 7 performs substantially the same functions as the selecting unit

610 of FIG. 6. Thus, the functions of the selecting unit 710 will not be explained again.

[0083] FIG. 8 illustrates a modified circuit diagram of the sense amplifying circuit illustrated in FIG. 6.

[0084] Referring to FIG. 8, a selecting unit 810 may include first and second switch transistors SWMN1 and SWMN2, and first and second inverted switch transistors ISWMN1 and ISWMN2, which have substantially the same structures as the first and second switches SWMN1 and SWMN2 and the first and second inverted switch transistors ISWMN1 and ISWMN2 of the selecting unit 710 of FIG. 7, and first and second select transistors SMN1 and SMN2 and first and second inverted select transistors ISMN1 and ISMN2 which are connected to the first and second switch transistors SWMN1 and SWMN2 and the first and second inverted switch transistors ISWMN1 and ISWMN2, respectively.

[0085] It is understood by those of ordinary skill in the art that the first and second select transistors SMN1 and SMN2 and the first and second inverted select transistors ISMN1 and ISMN2 of FIG. 8 have substantially the same functions as the first and second select transistors SMN1 and SMN2 of FIG. 6. Thus, the functions of the first and second select transistors SMN1 and SMN2 and the first and second inverted select transistors ISMN1 and ISMN2 of FIG. 8 will not be explained again.

[0086] FIG. 9 illustrates a circuit diagram of a bit comparator according to another exemplary embodiment of the present invention. Referring to FIG. 9, a bit comparator 900 may include a random access memory (RAM) cell 905, a selecting unit 910, a sensing unit 920, a latching unit 930, and an output unit 940.

[0087] The RAM cell 905 receives and stores data DATA and inverted data INDATA having an opposite level to the data DATA from a pair of data lines to generate a selection signal SEL and an inverted selection signal ISEL in response to a control signal CS.

[0088] In more detail, the RAM cell 905 includes a data maintainer 906 having first and second inverters ID1 and ID2, and first and second control transistors CMN1 and CMN2. Output of the first inverter ID1 is connected to input of the second inverter ID2, while input of the first inverter ID1 is connected to output

of the second inverter ID2. The first control transistor CMN1 transmits the data DATA to an input node of the first inverter ID1 via one of a pair of data lines in response to the control signal CS. The second control transistor CMN2 transmits the inverted data DATA to an input node of the second inverter ID2 via the other one of the pair of data lines in response to the control signal CS. The pair of data lines is a pair of bit lines BL and BLB.

[0089] The selecting unit 910 selects one pair from a first pair of first signal INH1 and first inverted signal INL1 and a second pair of second signal INH2 and second inverted signal INL2, in response to a first level of a clock signal CLK, the selection signal SEL, and the inverted selection signal ISEL.

[0090] The data DATA is equal to the selection signal SEL, and the inverted data INDATA is equal to the inverted selection signal ISEL. The first signal INH1 is identical to the second inverted signal INL2, and the second signal INH2 is identical to the first inverted signal INL1. The first signal INH1 has an opposite level to the first inverted signal INL1, and the first signal INH1 and the first inverted signal INL1 are address data input to the bit comparator 900.

[0091] The sensing unit 920 senses voltage levels of one pair selected from the first pair of first signal INH1 and first inverted signal INL1 and the second pair of second signal INH2 and second inverted signal INL2. When the clock signal CLK and the selection signal SEL are at a first level, in the sensing unit 920, a first sense transistor MN1 having a gate to which the first signal INH1 is applied and a first inverted sense transistor IMN1 having a gate to which the first inverted signal INL1 is applied are turned on, and a source of the first sense transistor MN1 is connected to a source of the first inverted sense transistor IMN1.

[0092] When the clock signal CLK and the inverted selection signal ISEL are at the first level, a second sense transistor MN2 having a gate to which the second signal INH2 is applied and a second inverted sense transistor IMN2 having a gate to which the second inverted signal INL2 is applied are turned on, and a source of the second sense transistor MN2 is connected to a source of the second inverted sense transistor IMN2.

[0093] The latching unit 930 precharges first and second nodes N1 and N2 in response to a second level of the clock signal CLK and controls voltage levels

of the first and second nodes N1 and N2 in response to a sensing result of the sensing unit 920.

[0094] The output unit 940 inverts the voltage levels of the first and second nodes N1 and N2 to generate first and second output signals OUTH and OUTL and determines in response to a level of the second output signal OUTL whether the data DATA and the inverted data INDATA coincide with the first signal INH1 and the first inverted signal INL1.

[0095] Hereinafter, the operation of the bit comparator 900 will be explained in detail with reference to FIG. 9.

[0096] As previously described with reference to FIG. 2, the general bit comparator 200 may generate the match signal by amplifying the input address data through the sense amplifying circuit 210 and the driver 220 and comparing the input address data with stored data. Thus, it takes a long time from input of the address data to output of the match signal.

[0097] In order to solve this problem, the bit comparator 900 of FIG. 9 uses a sense amplifying circuit according to an exemplary embodiment of the present invention instead of the sense amplifying circuit 210 of FIG. 2. The sense amplifying circuit according to an exemplary embodiment of the present invention is part of the bit comparator 900.

[0098] Address data input to the bit comparator 900 is a first pair of signals input to the sense amplifying circuit. The first pair of signals are inverted and then input as a second pair of signals to the sense amplifying circuit. The bit comparator 900 can reduce the time required for comparing the address data with data stored therein and amplifying the address data. Accordingly, a cache memory having the bit comparator 900 can operate at a high speed.

[0099] The operation of the bit comparator 900 of FIG. 9 will now be described. The RAM cell 905 receives the data DATA and the inverted data INDATA from the pair of bit lines BL and BLB via the first and second control transistors CMN1 and CMN2 and stores the data DATA and the inverted data INDATA in the data maintainer 906. When the first and second control transistors CMN1 and CMN2 are turned on in response to the control signal CS, the data DATA and the inverted data INDATA is applied to the data maintainer 906. The control signal CS is controlled by a word line WD.

[00100] The structures of the selecting unit 910, the sensing unit 920, the latching unit 930, and the output unit 940 are substantially equal to those of the sensing unit 610, the sensing unit 620, the latching unit 630, and the output unit 640. In other words, the comparator 900 of FIG. 9 includes a combination of the sense amplifying circuit 600 and the RAM cell 905.

[00101] When the data DATA is at a low level and the inverted data INDATA is at a high level, the data DATA is applied as the selection signal SEL to a first select transistor SMN1 and the inverted data INDATA is applied as the inverted selection signal ISEL to a second select transistor SMN2.

[00102] When the clock signal CLK is at a high level, the second select transistor SMN2 is turned on. Thus, the second sense transistor MN2 having the gate to which the second signal INH2 is applied and the second inverted sense transistor IMN2 having the gate to which the second inverted signal INL2 is applied are turned on.

[00103] When the voltage level of the first signal INH1 is higher than the voltage level of the first inverted signal INL1, since the second inverted signal INL2 is equal to the first signal INH1, the second inverted sense transistor IMN2 allows a larger amount of current to flow than the second sense transistor MN2. Thus, a voltage level of the second node N2 becomes lower than a voltage level of the first node N1. The output unit 940 outputs the second output signal OUTL having a higher voltage level than the first signal OUTH.

[00104] A high level of the second output signal OUTL of the first and second output signals OUTH and OUTL of the bit comparator 900 indicates that the data DATA and the inverted data INDATA stored in the RAM cell 905 have a different level from the first signal INH1 and the first inverted signal INL1 input to the bit comparator 900, i.e., the address data.

[00105] In contrast, a low level of the second output signal OUTL indicates that the data DATA and the inverted data INDATA stored in the RAM cell 905 have the same level as the first signal INH1 and the first inverted signal INL1 input to the bit comparator 900, i.e., the address data.

[00106] In the above example, when the second output signal OUTL is at the high level, the address data input to the bit comparator 900, i.e., the first

signal INH1 and the first inverted signal INL1, does not coincide with the data DATA and the inverted data INDATA stored in the data maintainer 906.

[00107] As described above, the bit comparator 900 of FIG. 9 includes the sense amplifying circuit according to an exemplary embodiment of the present invention. Thus, compared to the bit comparator 200, the bit comparator 900 can considerably reduce the time required for comparing address data with stored data.

[00108] The bit comparator 900 of FIG. 9 includes a combination of the RAM cell 905 and the sense amplifying circuit 600 of FIG. 6. However, it will be understood by those of ordinary skill in the art that the bit comparator 900 may include a combination of the RAM cell 905 and the sense amplifying circuit 700 of FIG. 7 or a combination of the RAM cell 905 and the sense amplifying circuit 800 of FIG. 8.

[00109] FIG. 10 illustrates a modified circuit diagram of the bit comparator of FIG. 9.

[00110] A bit comparator 1000 of FIG. 10 includes a combination of a RAM cell and the sense amplifying circuit 300 of FIG. 3. It is obvious to those of ordinary skill in the art that the operation of the bit comparator 1000 is substantially the same as the operation of the bit comparator 900 of FIG. 9. Thus, details of the operation of the bit comparator 1000 will not be described herein.

[00111] The bit comparator 1000 of FIG. 10 includes the combination of the RAM cell and the sense amplifying circuit 300 of FIG. 3. However, it is understood by those of ordinary skill in the art that the bit comparator 1000 may include a combination of the RAM cell and the sense amplifying circuit 400 of FIG. 4 or a combination of the RAM cell and the sense amplifying circuit 500 of FIG. 5.

[00112] FIG. 11 illustrates a block diagram for explaining the bit comparators of FIGS. 9 and 10.

[00113] A bit comparator 1100 (each of the bit comparators 900 and 1000 of FIGS. 9 and 10) includes a combination of a RAM cell 1110 and a sense amplifying circuit 1120. The RAM cell 1110 receives and stores data DATA and inverted data INDATA from a pair of bit lines BL and BLB in response to a control signal controlled by a word line WD, and outputs the

data DATA and the inverted data INDATA as a selection signal SEL and an inverted selection signal ISEL, respectively.

[00114] The sense amplifying circuit 1120 receives a first signal INH1, a first inverted signal INL1, a second inverted signal INL2 into which the first signal is inverted, and a second signal INH2 into which the first inverted signal INL1 is inverted, and selects the first signal INH1 and the first inverted signal INL1 or the second signal INH2 and the second inverted signal INL2 in response to the selection signal SEL.

[00115] The bit comparator 1100 compares voltage levels of the selected signals with voltage levels of the data DATA and the inverted data INDATA to output first and second output signals OUTH and OUTL. The comparator 1100 determines in response to the voltage level of the second output signal OUTL whether the data DATA and the inverted data INDATA stored in the RAM cell 1110 coincide with address data input to the comparator 1100, i.e., the first signal INH1 and the first inverted signal INL1.

[00116] The sense amplifying circuit 1120 may be one of the sense amplifying circuits 300, 400, 500, 600, 700, and 800 of FIGS. 3, 4, 5, 6, 7, and 8.

[00117] As described above, a sense amplifying circuit according to an exemplary embodiment of the present invention may receive two pairs of differential signals, selects one pair of differential signals from the two pairs of differential signals, and amplifies only the selected pair of differential signals. As a result, a significant logic burden is normally not imposed on a rear end of the sense amplifying circuit. In addition, a bit comparator having the sense amplifying circuit according to an exemplary embodiment of the present invention may generally operate at a high speed. Thus, a high-speed cache memory can be realized.

[00118] While the present invention has been described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as defined by the claims.